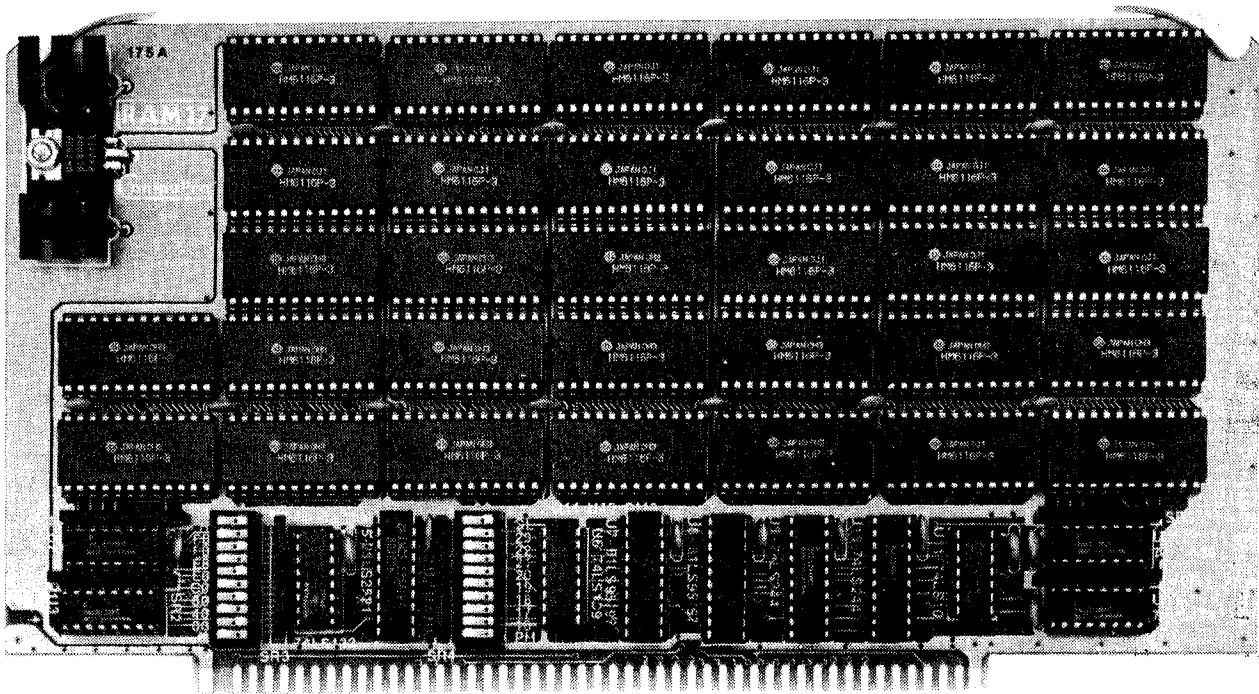


# RAM 17™

## TECHNICAL MANUAL



IEEE 696 / S-100

# 64K STATIC MEMORY



**CompuPro™**

division

**GODBOUT**  
ELECTRONICS

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## TECHNICAL OVERVIEW

The **RAM 17** is a 64K static RAM board designed especially for multi-user systems where speed, density, reliability and low-power are at a premium. Using Hitachi 6116 CMOS `byte-wide` 16K RAM's, the **RAM 17** can be configured as an Extended Address board (compatible with the 8088 CPU or with Godbout memory management hardware), or as Global memory. When used in conjunction with a Compupro CPU or Memory Manager board, the **RAM 17** can be treated in software as a conventional Bank Select board

The **RAM 17** is configured as a single 64K block beginning at any 64K address within the entire 24 bit (16 Megabyte) address range specified for the S-100 bus by IEEE spec 696. Four 16K segments may be individually disabled through an on-board DIP switch, and the highest 8K block (E000H-FFFFH) is further divided into four 2K blocks which may also be individually switch disabled. This allows the use of The **RAM 17** with a broad selection of memory mapped devices such as disk controllers and video boards. This `windowing` ability also allows a multi-user system to have a single `Global` board plus a number of partially populated **RAM 17**'s (e.g., one for each user.)

The **RAM 17** is shipped as a 48K or 64K board. Partially populated boards may be upgraded simply by inserting additional 6116 RAM IC's into pre-installed DIP sockets (all boards come with all 32 RAM IC sockets wave soldered in place.) Extra heavy duty power traces, generous bypassing of supply lines, sockets for all integrated circuits, careful layout, innovative design conservatively implemented, premium parts, and a double sided, solder-masked printed circuit board with complete component legends make this a versatile, dependable, high performance memory board.

Since RAM memory is one of the most expensive components in any S-100 installation, using the **RAM 17** as the heart of a system insures that the transition to faster CPU's and/or more sophisticated memory management software will be as easy and inexpensive as possible. Because of the board's extremely low power consumption (populated to 64K these boards draw less than 200 milliamps), numerous **RAM 17**'s can be combined without exceeding the capacity of the system power supply. Because of the board's high density, large amounts of RAM (up to a megabyte) can be configured in a single system without running out of card slots. Since the **RAM 17** is guaranteed to run with 6 Mhz Z-80's and 10 Mhz 8086/88's, upgrading to faster CPU's will not threaten your investment in memory. And because the **RAM 17** uses static RAM memory, the user is assured of long, reliable operation and easy maintenance.

The **RAM 17** conforms fully to IEEE spec 696.

## RAM 17 SWITCH FUNCTIONS

The RAM 17 uses 2K x 8 IC's to provide 64K of memory. The user has the option of setting the board to decode either 16 address lines (Global Mode) or 24 address lines (Extended Mode). The board is permanently addressed with respect to the lower 16 address lines (A0-A15), always occupying XX0000H - XXFFFFH (where 'XX' represents address lines A16-A23). The board may not be addressed to cross a lower 16 bit, 64K boundary. Thus, two fully populated RAM 17's addressed consecutively in Extended Mode to occupy the lowest legal address interval would span from 000000H to 01FFFFH. A RAM 17 may not be addressed to span from, say, 008000H to 017FFFH, as this would cross a 64K address boundary.

When switched to run in Extended Mode, the RAM 17 will perform a full 24 bit address decode, including the 8 extended address lines (A16-A23). This allows as many as 256 RAM 17's in a system without causing an addressing conflict.

The RAM 17 may be set to become disabled when the PHANTOM line (S-100 line 67) is asserted. The Two 10 position DIP switches on the RAM 17 are used to select all of the user selectable board options. These switches are described below.

### SWITCH S1 - BLOCK ENABLE, FRONT PANEL/STANDARD MODE SELECT

Switch S1 paddles 6 through 9 allow the user to selectively enable or disable any of the four 16K blocks which comprise the RAM 17. S1 paddles 2 through 5 allow the the user to selectively enable or disable the four 2K blocks which make up the last half (XXE000H to XXFFFFH) of the fourth 16K block. Setting any paddle 'ON' enables its associated block, while setting any paddle 'OFF' disables its associated block. Disabling a block frees its address space for use by off-board memory devices. The relationship between paddle number and block location and size is illustrated below. (The starting block location controlled by each paddle is indicated on the legend on the P.C. board just to the left of Switch S1.

### SWITCH S1 : BLOCK ENABLE - PADDLES 2 - 9

	PADDLE NUMBER	ASSOCIATED BLOCK IN HEX (lower 16 bit extent)
'ON' enables	9 .....	0000 - 3FFF
associated block	8 .....	4000 - 7FFF
	7 .....	8000 - BFFF
	6 .....	C000 - FFFF

Paddle 6 must be "ON" for paddles 2-5 to take effect

'ON' enables	5 .....	E000 - E7FF
associated block	4 .....	E800 - EFFF
	3 .....	F000 - F7FF
	2 .....	F800 - FFFF

For example, to disable the first 16K of RAM (from XX0000H - XX3FFFH) as well the 2K block from XXE000H to XXE7FFFH, paddles 5 and 9 of Switch S1 should be turned 'OFF' and paddles 2-4 and 6-8 should be turned 'ON'.

Note that the lower 16 bit starting address for the **RAM 17** is always 0000H. Paddles 2 - 9 of Switch S2 do NOT allow the user to address the **RAM 17**, but simply allow the user to create 'windows' within a 64K block whose lower 16 bits have been permanently addressed.

For the correspondence between **RAM 17** lower 16 bit addresses and the physical location of the thirty-two on-board 24 pin IC sockets, see the picture of the PC board at the back of the manual. Each 24 pin memory IC location shown on this picture contains two characters representing the starting address of the 2K block controlled by the IC in question. Thus, the IC in the location marked 'C8' controls memory from XXC800H - XXCFFFH, the IC in the location marked '20' controls XX2000H - XX27FFH, etc.

**SWITCH S1 : NORMAL/FRONT PANEL MODE SELECT - PADDLES 1 & 10**

Switch S1 paddles 1 and 10 are used to set the **RAM 17** to operate in Normal or Front Panel mode. Placing Switch S1 paddle 10 'OFF' and paddle 1 'ON' selects Front Panel Mode. Placing paddle 10 'ON' and paddle 1 'OFF' selects Normal Mode. In Front Panel Mode the **RAM 17** can be written to using an IMSAI type front panel. NEVER SWITCH BOTH OF THESE PADDLES TO THE SAME POSITION!

An IMSAI front panel write operation depends upon an illegal status condition which will not work reliably with devices which, like the **RAM 17**, use an internal bi-directional data bus. By selecting Front Panel Mode, this illegal status condition is accepted by the **RAM 17**, although the bandwidth of the board's write timing is significantly narrowed. Because of this write timing degradation, the **RAM 17** should not be run in Front Panel Mode unless front panel operation is required-- e.g., for diagnostic purposes. Timing guarantees offered with this board assume operation with Switch S1-10 turned 'ON' and S1-1 turned 'OFF'.

The use of paddles 1 and 10 of Switch S1 is illustrated below:

**SWITCH S1 : PADDLES 1 & 10**

	PADDLE NUMBER	FUNCTION
'ON' SELECTS	1 .....	FRONT PANEL MODE
MODE	10 .....	NORMAL MODE

Paddles 1 and 10 must never both be 'ON' or both be 'OFF'!

**SWITCH S2, PADDLE 1 : GLOBAL ENABLE**

Switch S2 paddle 1 is used to set the addressing mode of the **RAM 17** to Global or Extended. If this switch is put in the 'ON' position, the **RAM 17** will become Global memory, i.e., it will respond to ALL memory addresses not disabled by Switch S1. Setting S2 paddle 1 to 'OFF' puts the **RAM 17** in Extended Mode, i.e., it will perform a full 24 bit address decode before becoming selected. WHEN RUNNING THE **RAM 17** IN GLOBAL MODE THE 25LS2521 IC AT LOCATION U5 MUST BE REMOVED.

The use of paddle 1 of Switch S2 is illustrated on the following page:

**SWITCH S2-1 GLOBAL MODE ENABLE**

PADDLE NUMBER	FUNCTION
1 .....	GLOBAL ENABLE
	`ON` selects Global Mode (IC U5 NOT installed)
	`OFF` Selects Extended Mode (IC U5 installed)

**SWITCH S2, PADDLES 2-9 : EXTENDED ADDRESS MODE**

If S2 paddle 1 is switched `OFF`, the RAM 17 will be in Extended Mode. In this case, paddles 2 through 9 of Switch S2 must be set so as to establish the extended memory page which the board is to occupy. In Global Mode, with S2 paddle 1 `ON`, these switches are of no consequence. IN EXTENDED MODE, IC U5 MUST BE INSTALLED.

**SWITCH S2 2-9 : EXTENDED ADDRESSING**  
(S2-1 must be `OFF`; IC U5 must be installed)

	PADDLE NUMBER	EXTENDED ADDRESS LINE
`ON` = `0` does not match bit	2 .....	A23 (bus pin 64)
	3 .....	A22 (bus pin 63)
	4 .....	A21 (bus pin 62)
	5 .....	A20 (bus pin 61)
	6 .....	A19 (bus pin 59)
`OFF` = `1` matches bit	7 .....	A18 (bus pin 15)
	8 .....	A17 (bus pin 17)
	9 .....	A16 (bus pin 16)

Thus, to set the RAM 17 to reside in extended page 80XXXXH, paddle 2 of S2 should be turned `OFF`, and paddles 3 - 9 should be turned `ON`.

**SWITCH S2, PADDLE 10 : PHANTOM ENABLE**

Switch S2 paddle 10 allows the assertion of the PHANTOM line (S-100 line 67) to disable the RAM 17. When PHANTOM is asserted (low) and S2 paddle 10 is set to `ON`, the on board RAM can not be read or written. This applies to ALL addressing modes. Many S-100 Power-on-Jump circuits rely on the ability of system RAM to be disabled by the PHANTOM line, as do a number of Interrupt Controller boards. Setting S2 paddle 10 `OFF` will cause the RAM 17 to disregard PHANTOM.

The use of paddle 10 of Switch S2 is illustrated below:

**SWITCH S2 : PADDLE 10**

PADDLE NUMBER	FUNCTION
10 .....	PHANTOM ENABLE
	Should be `ON` for normal operation in most systems.

## APPENDIX

### RAM 17 ADDRESSING MODES

Two addressing modes are supported by the RAM 17:

1. Global
2. Extended Address

The RAM 17 must be assigned one of these two modes. Within a given RAM 17, only one mode is possible (e.g., one cannot have half the board Global and the other half Extended Address), but it is possible to configure a SYSTEM with a combination of Global, Extended Address and even Bank Select boards. These two modes are selected both through switch settings and by installing or not installing a 25L2521 IC in socket U5. In Global mode, IC U5 must NOT be installed. In Extended mode, U5 must be installed.

### DEFINITION OF A MEMORY PAGE

When this manual refers to a Page NN of memory, it means a 64K byte block beginning at NN0000H and ending at NNFFFFH. Since IEEE spec 696 defines 24 address lines, there are 256 possible 64K pages on the S-100 bus. Each page is uniquely identified by the 8 highest address lines (the 'Extended Address' lines), A16-A23. Thus, Page 0 (Base Page) extends from 000000H to 00FFFFH, Page 1 from 010000H to 01FFFFH, etc.

### GLOBAL MODE (Switch S2, Paddle 1 'ON') (IC U5 NOT installed)

Global memory is memory that occupies all pages. In Global Mode, the RAM 17 will respond only to the lower 16 S-100 address lines (A0-A15), ignoring the upper 8 lines (A16-A23) and disregarding any I/O instructions. Global memory boards allow an area of memory that is common to all pages-- a necessity for conventional Bank Select schemes. Global memory also limits the amount of non-global memory available in any page, since the lower 16 bits of Extended Address or Bank Select memory must not conflict with the system's global memory. Thus if a Global board is addressed from 0000H to 3FFFH (the first 16K), then the lower 16 bit addressing of any Extended Address or Bank Select board in the system must fall between 4000H and FFFFH, limiting each non-global board in this example to a maximum of 48K.

The maximum Global memory possible in a system is 64K.

### EXTENDED ADDRESS MODE COMPATIBILITY WITH BANK SELECT SOFTWARE

(Switch S2, paddle 1 'OFF'-- IC U5 installed)

Extended Address memory occupies a single 64K page and no other. In Extended Address mode, the RAM 17 will decode all 24 address lines in order to become selected. Although all 8 bit S-100 CPU boards will generate the lower 16 address bits (A0-A15), few other than CompuPro CPU's are capable of generating the additional 8 address bits A16-A23. In order to generate these 8 extra address bits in a system driven by an 8 bit CPU, some type of 'memory manager' device is required.

## Memory Managers

For our purposes, a memory manager is any device capable of driving address lines which the CPU cannot drive. CompuPro produces CPU boards with built-in memory management circuitry, and a stand-alone Memory Manager board is available for systems not using CompuPro CPU's. CompuPro memory managers can be made to generate address bits A16-A23 through the following software mechanism:

- 1: Assign the Memory Manager an I/O port number
- 2: Output the 64K page number to the memory manager port

As an example, suppose that an Extended Address memory board is addressed to Page 5 (05XXXXH), and the Memory Manager is addressed to I/O port FDH. The following 8080 assembly code will qualify this Extended Address memory board for selection:

```
3E05  MVI    A,5H    ;page number into accumulator
D3FD  OUT    OFDH   ;output to memory manager port
```

This sequence would cause the Memory Manager to latch the contents of the accumulator (in this case a 5H) onto the Extended Address lines (A16-A23), and preserve these lines in this state until they are changed by a subsequent output to the Memory Manager port or by a system reset. Specifically, Extended Address lines A16 and A18 would be latched high, while the other six Extended Address lines would be latched low.

The above software mechanism is compatible with that used by conventional 'Bank Select' schemes. In fact, it would be impossible to tell from a software standpoint whether a 'Bank Select' system using a single I/O port address were implemented with Bank Select boards, Extended Address boards plus a Memory Manager, or a combination of both.

The maximum Extended Address memory available in a system is 256 times 64K, or 16 Megabytes.



**SWITCH SETTINGS AT A GLANCE**  
(see Manual for Complete Description)

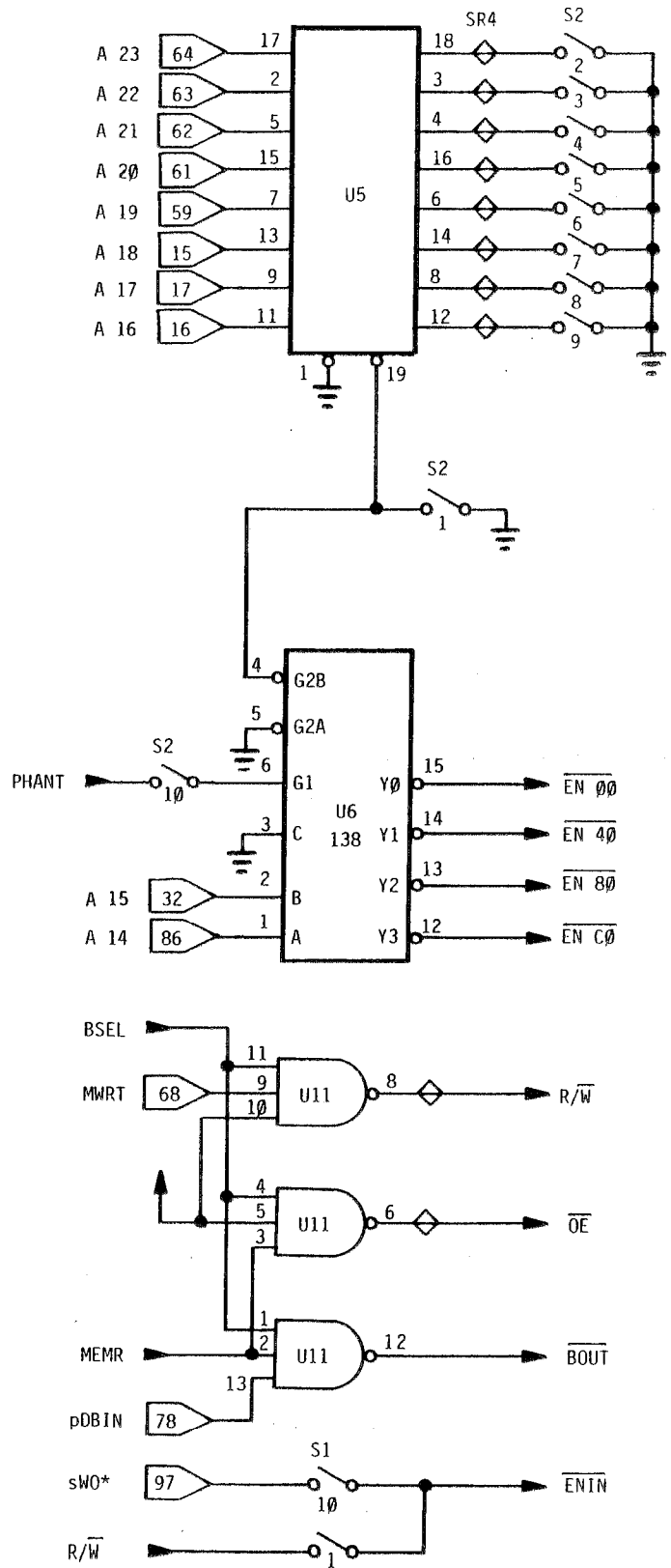
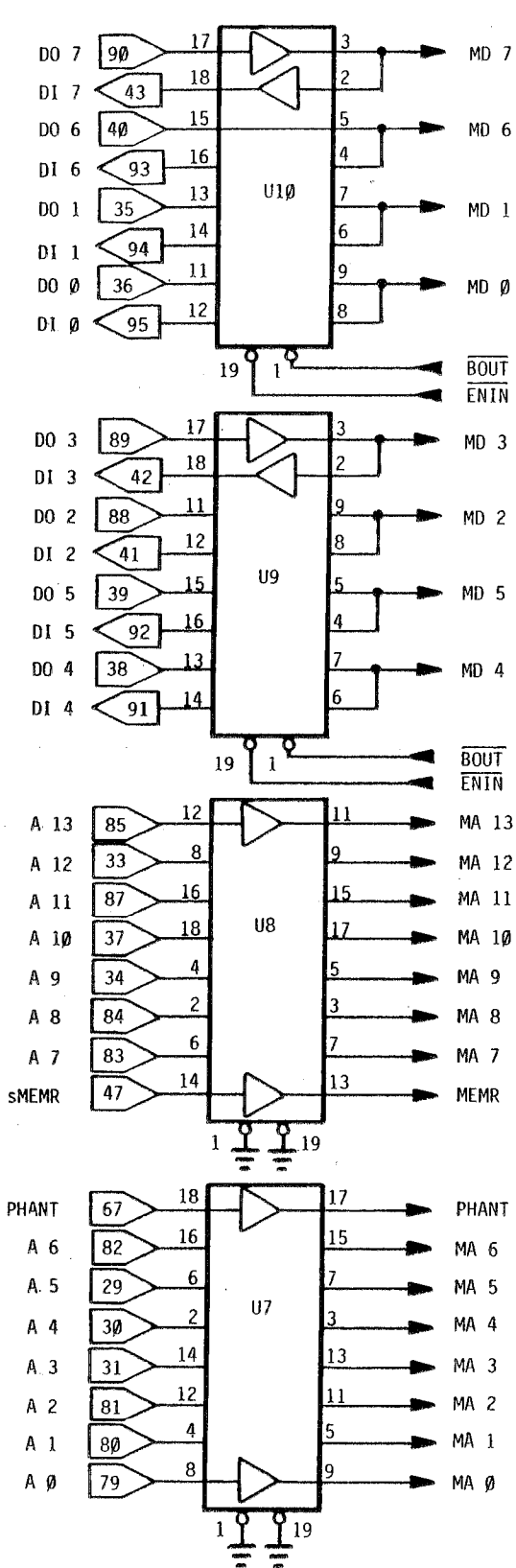
Front Panel			Global Enable			
Mode Enable*						'ON' for Global
		1			1	
B	F800-FFFF	2		A23	2	
L	F000-F7FF	3	'ON' enables	A22	3	'ON'
O			block	A		'ON' clears
C	E800-EFFF	4		E D	4	address
K				X D		bit to 0
E<	E000-E7FF	5	'OFF' disables	T R	5	
N	C000-FFFF	6	block	E E <		'OFF' sets
A				N S	6	address
B	8000-BFFF	7		D S	7	bit to 1
L				E I		
E	4000-7FFF	8		D N	8	
				G		
	0000-3FFF	9			9	
Normal Mode Enable*		10		Phantom Enable	10	'ON' for normal operation

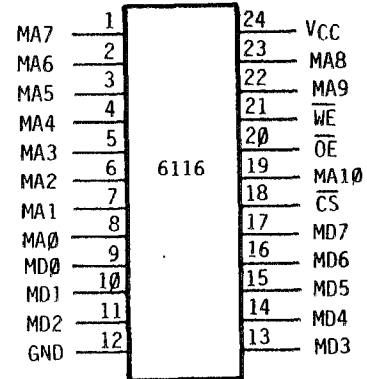
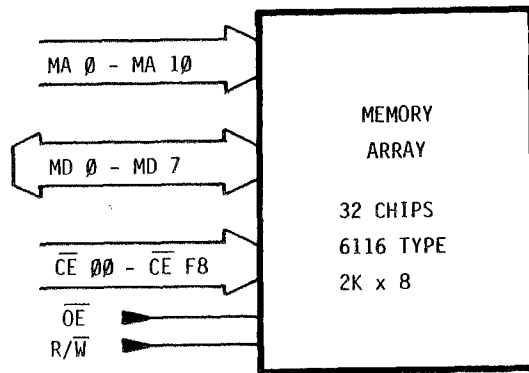
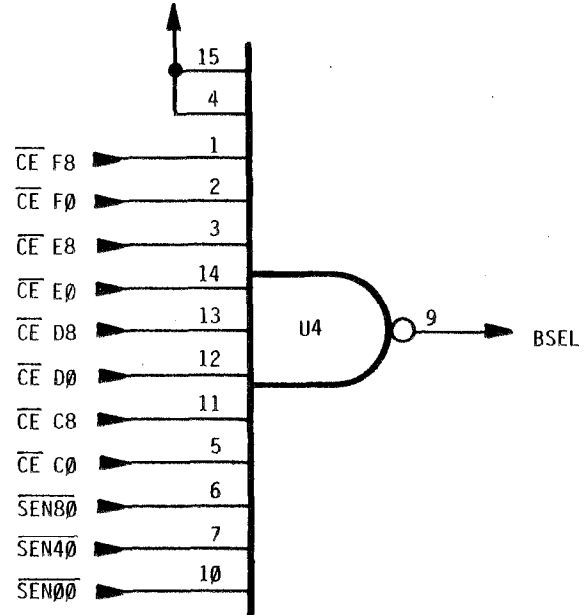
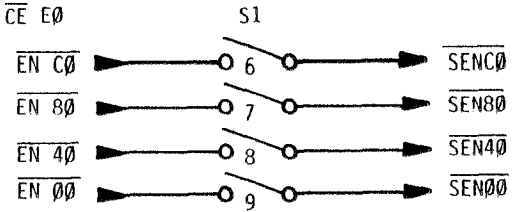
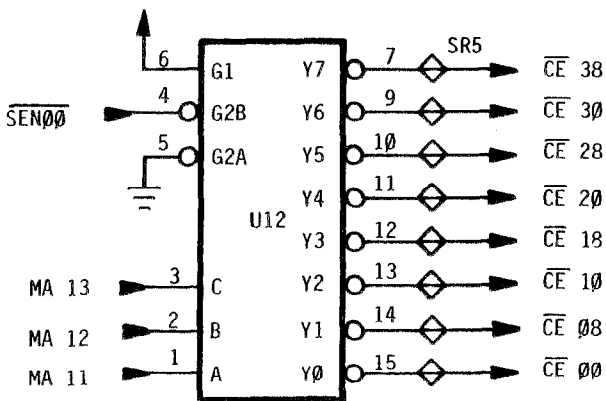
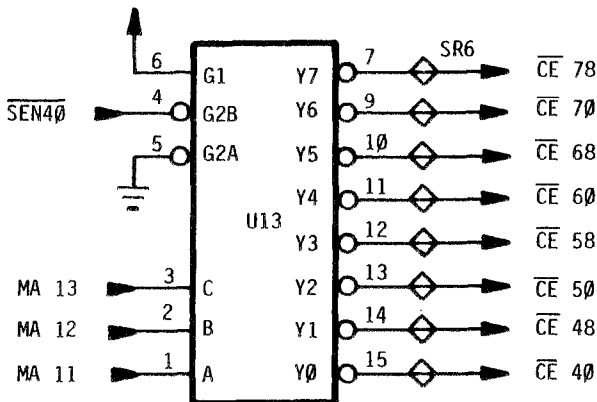
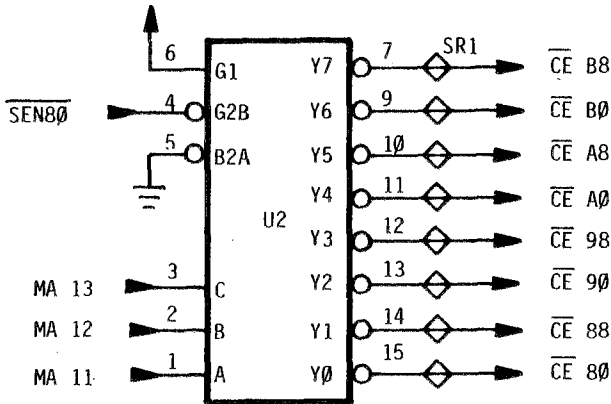
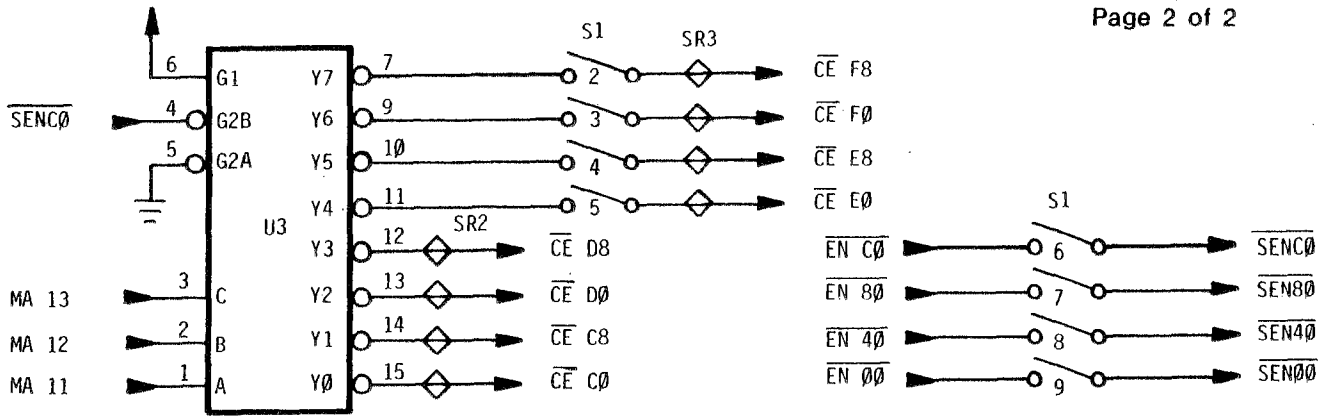
In Global mode, IC U5 must NOT be installed.

In Extended mode, IC U5 must be installed.

\*When using an IMSAI type front panel to write manually into RAM 17 memory, S1-10 should be turned 'OFF' and S1-1 should be turned 'ON'. When running programs, even in systems with an IMSAI front panel, S1-10 should be turned 'ON' and S1-1 should be turned 'OFF'. NEVER HAVE S1-1 AND S1-10 BOTH TURNED ON OR BOTH TURNED OFF!







## PARTS LIST

INTEGRATED CIRCUITS (note: the following parts may have letters, suffixes and prefixes along with the key characters given below:

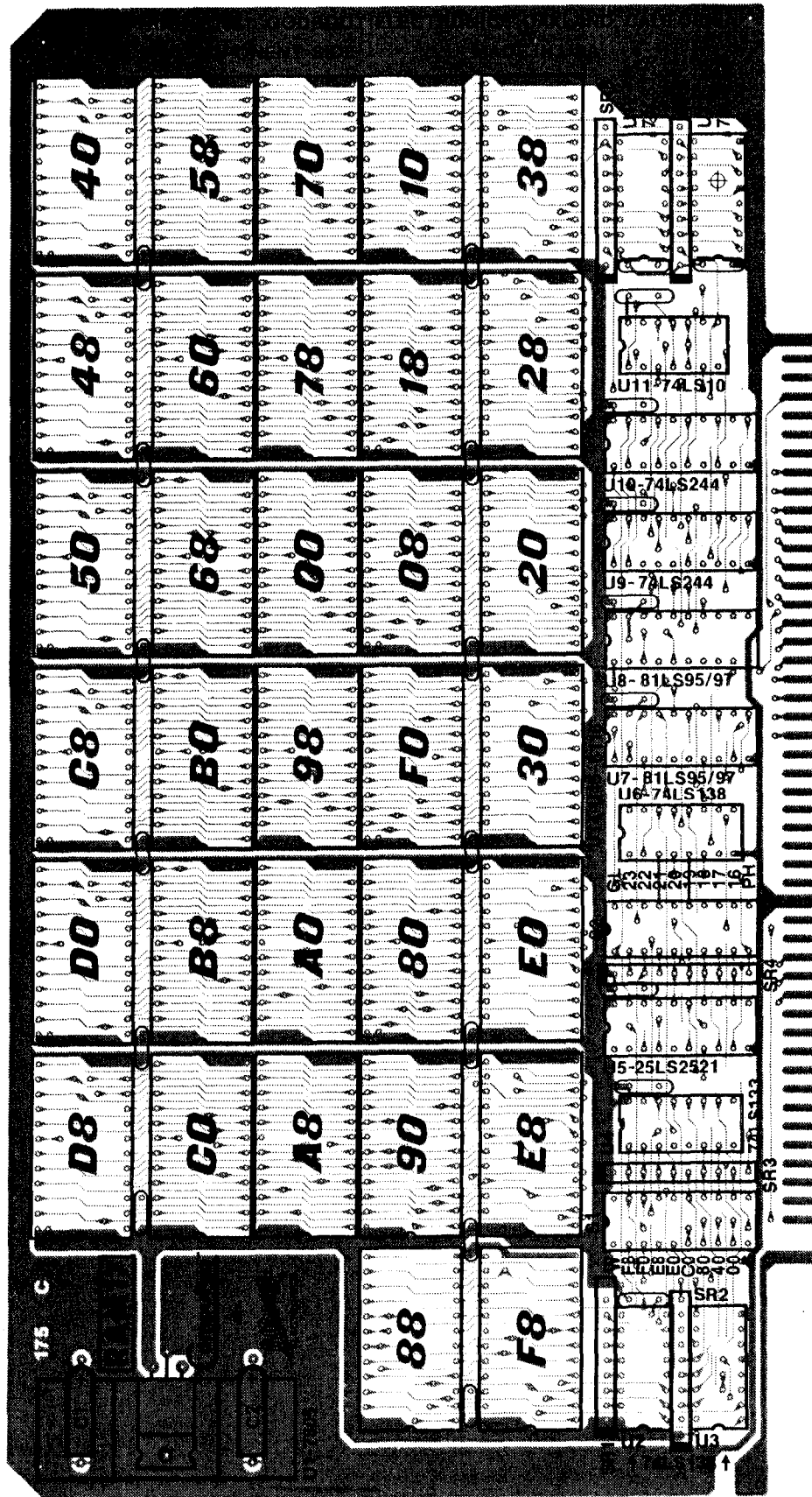
(32)	6116	2K x 8 CMOS static RAM	(U14-U45)
(1)	74LS10	triple 3 input NAND	(U11)
(1)	74LS133	13 input NAND	(U4)
(5)	74LS138	decoder	(U2,U3,U6,U12,U13)
(2)	74LS244	octal Tri-State® buffer	(U9,U10)
(2)	81LS95/97	octal bus driver	(U7,U8)
(1)	25LS2521	octal comparator	(U5)
(1)	7805	5 volt regulator	(U1)

### OTHER ELECTRONIC COMPONENTS

(2)	10 pin 4.7K-5.1K SIP resistor pack	(SR3,SR4)
(4)	10 pin 2.7K-5.1K SIP resistor packs	(SR1,SR2,SR5,SR6)
(2)	Tantalum capacitors	(C1,C2)
(23)	Ceramic bypass capacitors	

### MECHANICAL COMPONENTS

(44)	Low profile sockets	
(2)	DIP switch, 10 position	(S1,S2)
(1)	T0-220 heatsink	
(1)	Set 6-32 hardware	



COMPONENT LAYOUT

IF YOU NEED ASSISTANCE ALWAYS CONTACT  
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If you need further information feel free to write us at:

**Box 2355, Oakland Airport, CA 94614-0355**

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If a defective part causes a Godbout Electronics product to operate improperly during the 1 year warranty period, we will service it free (original owner only) if delivered and shipped at owner's expense to and from Godbout Electronics. If improper operation is due to an error or errors on the part of the purchaser, there may be a repair charge. Purchaser will be notified if this charge exceeds \$50.00.

We are not responsible for damage caused by the use of solder intended for purposes other than electronic equipment construction, failure to follow printed instructions, misuse or abuse, unauthorized modifications, use of our products in applications other than those intended by Godbout Electronics, theft, fire, or accidents.

Return to purchaser of a fully functioning unit meeting all advertised specifications in effect as of date of purchase is considered to be complete fulfillment of all warranty obligations assumed by Godbout Electronics. This warranty covers only products marketed by Godbout Electronics and does not cover other equipment used in conjunction with said products. We are not responsible for incidental or consequential damages.

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"TRI-STATE" is a trademark of National Semiconductor Corp.

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